**Lab 3 – Ripple Carry Adder**

**Name : Chirath A.A.I**

**Index No : 210086E**

* Lab Tasks :

The results of this lab were designing a Half Adder, utilizing the Half Adder to develop a Full Adder, and then using the Full Adder to design the 4-bit Ripple Carry Adder. Finally, we must use the BAYSIS 3 development board to simulate and test the RCA's performance.

* Truth Tables and Boolean Expressions:

1). Half Adder

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | S | C |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

Sum(S) 🡪 A B

Carry(C) 🡪 A . B

2). Full Adder

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | Cin | S | Cout |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

Sum(S) 🡪 A’B’Cin + A’BCin’ + AB’Cin’ + ABCin

= (A’B’ + AB) Cin + (A’B+ AB’) Cin’

= (A B)’ Cin +(A B) Cin’

= (A B) Cin

= A B Cin

Carry Out(Cout) 🡪 A’BCin + AB’Cin + ABCin’ + ABCin

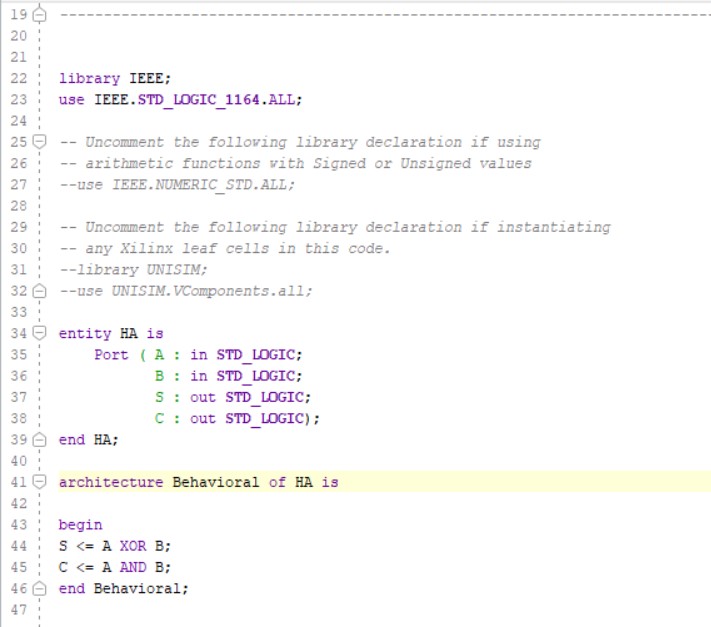
= (B’Cin + BCin’)A + BCin(A’ + A)

= A(B Cin) + BCin(1)

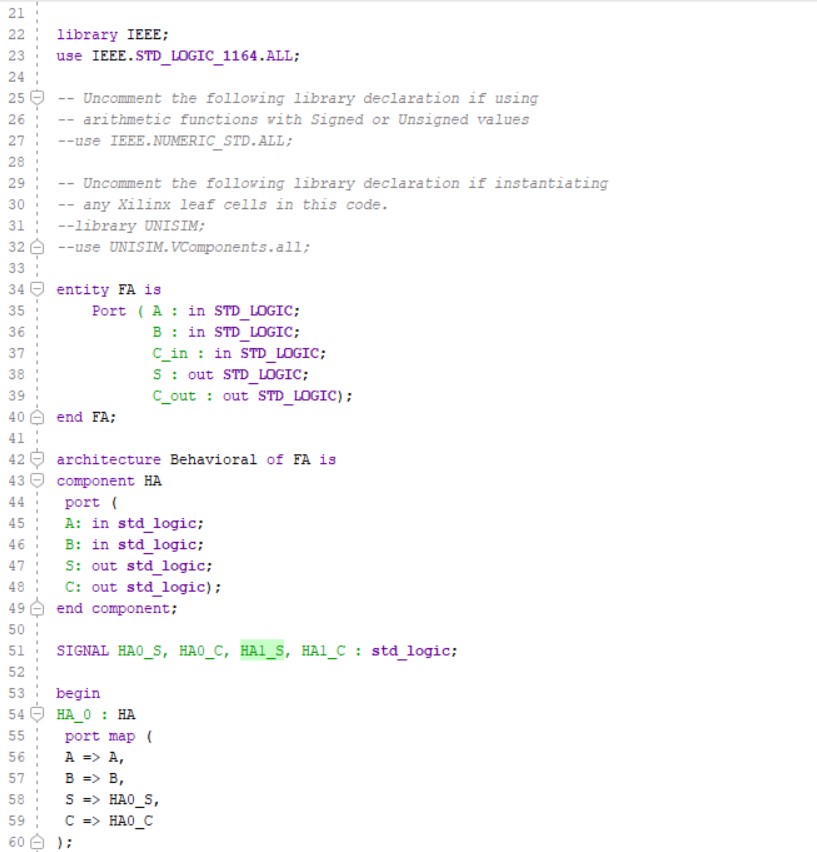
= A(B Cin) + BCin

VHDL Files: -

1). Half Adder



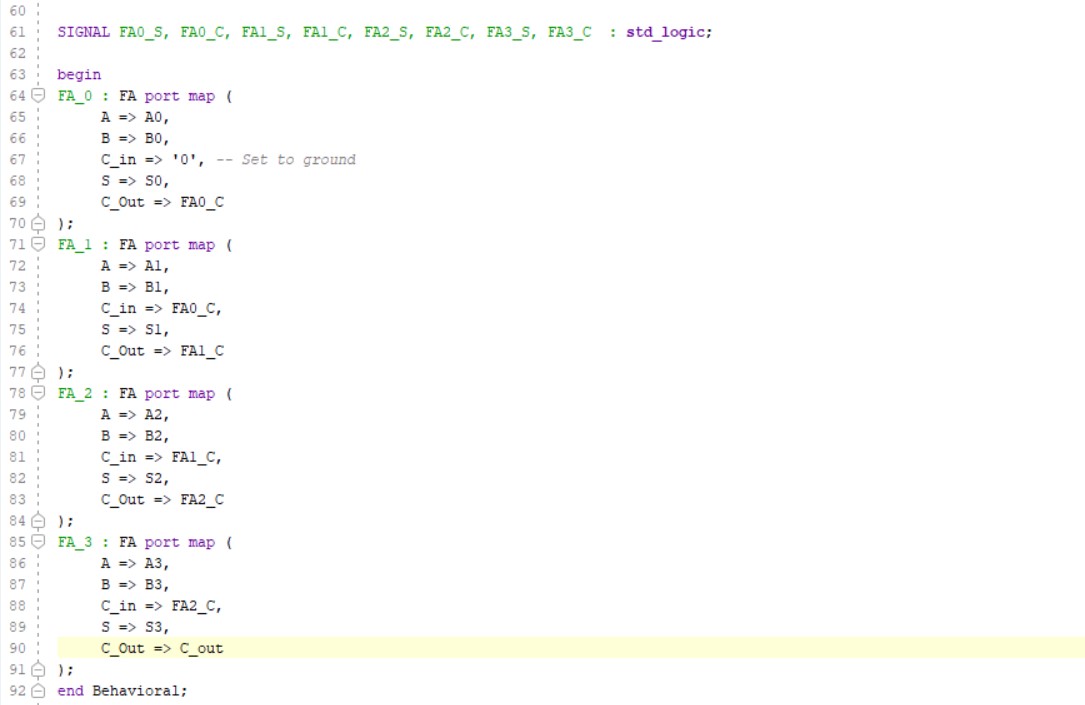
2). Full Adder





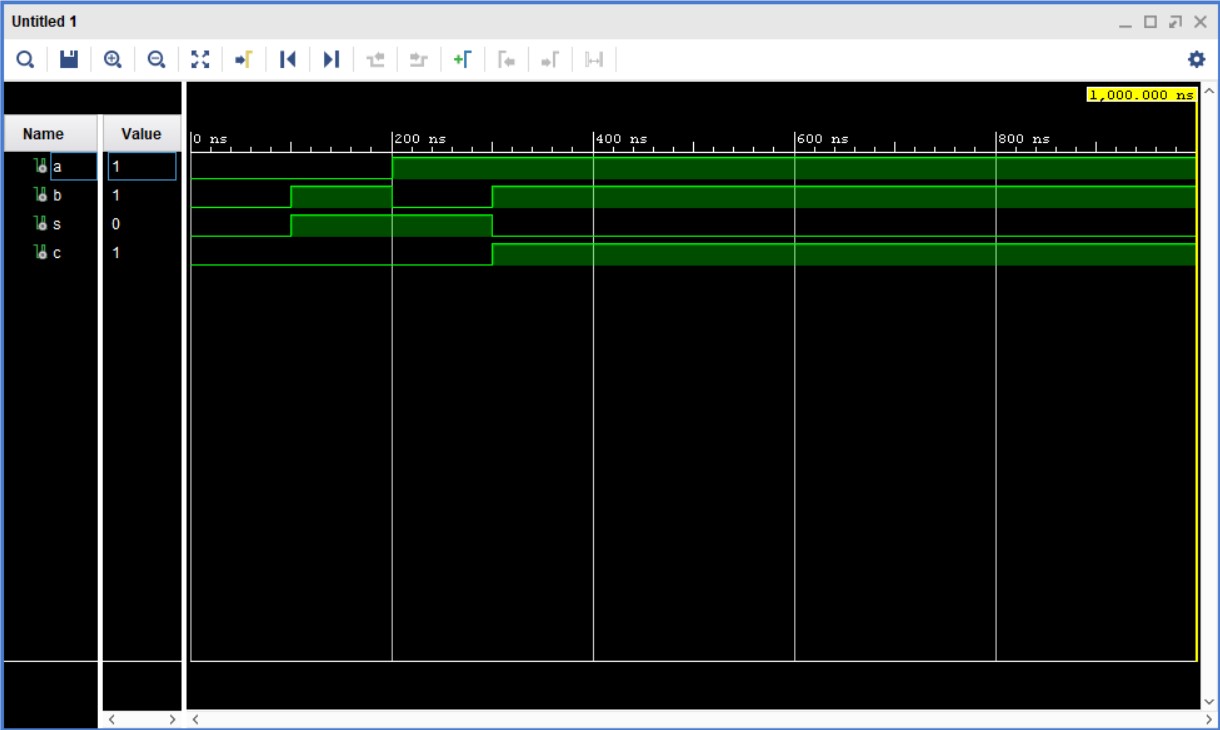
3). 4-Bit RCA



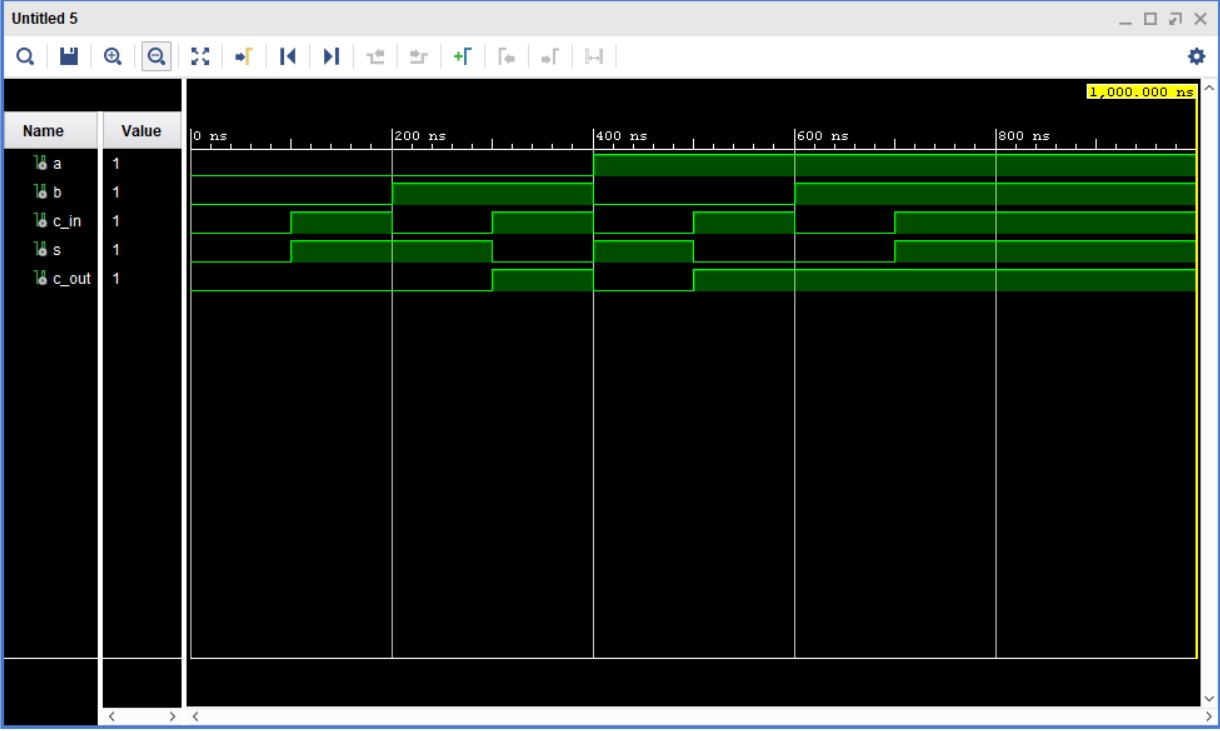


Timing Diagrams : -

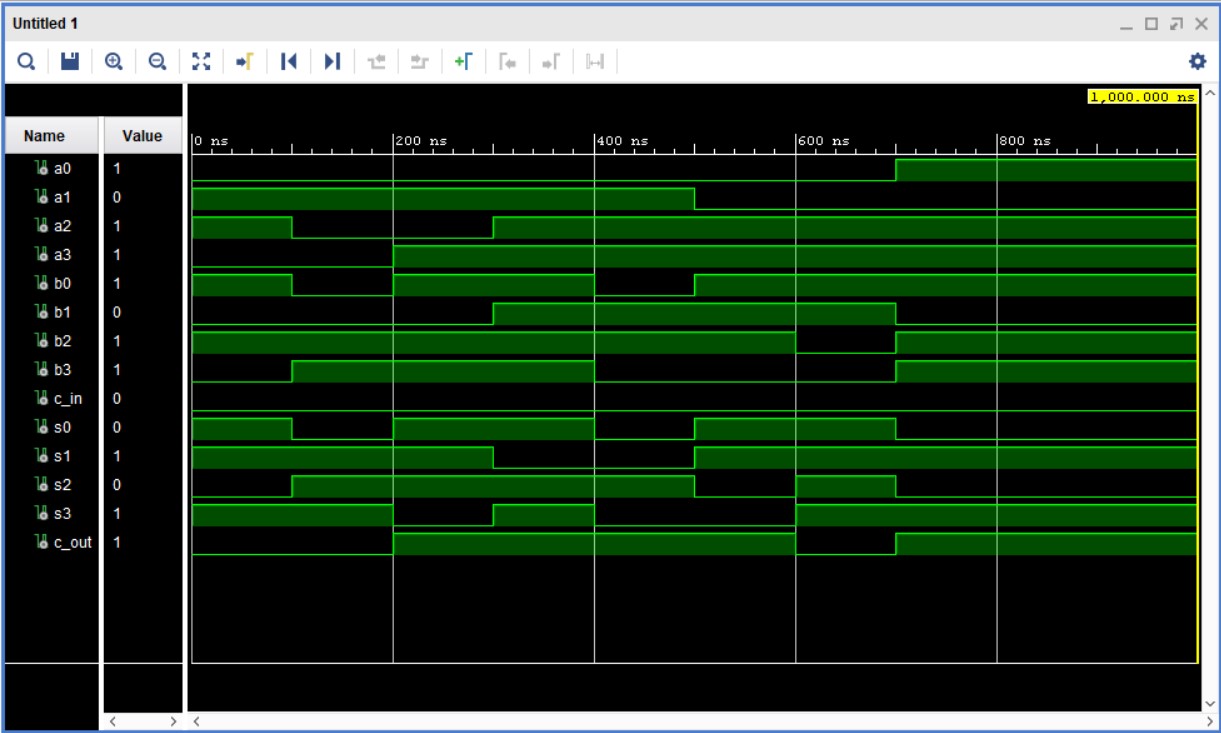
1). Half Adder



2). Full Adder

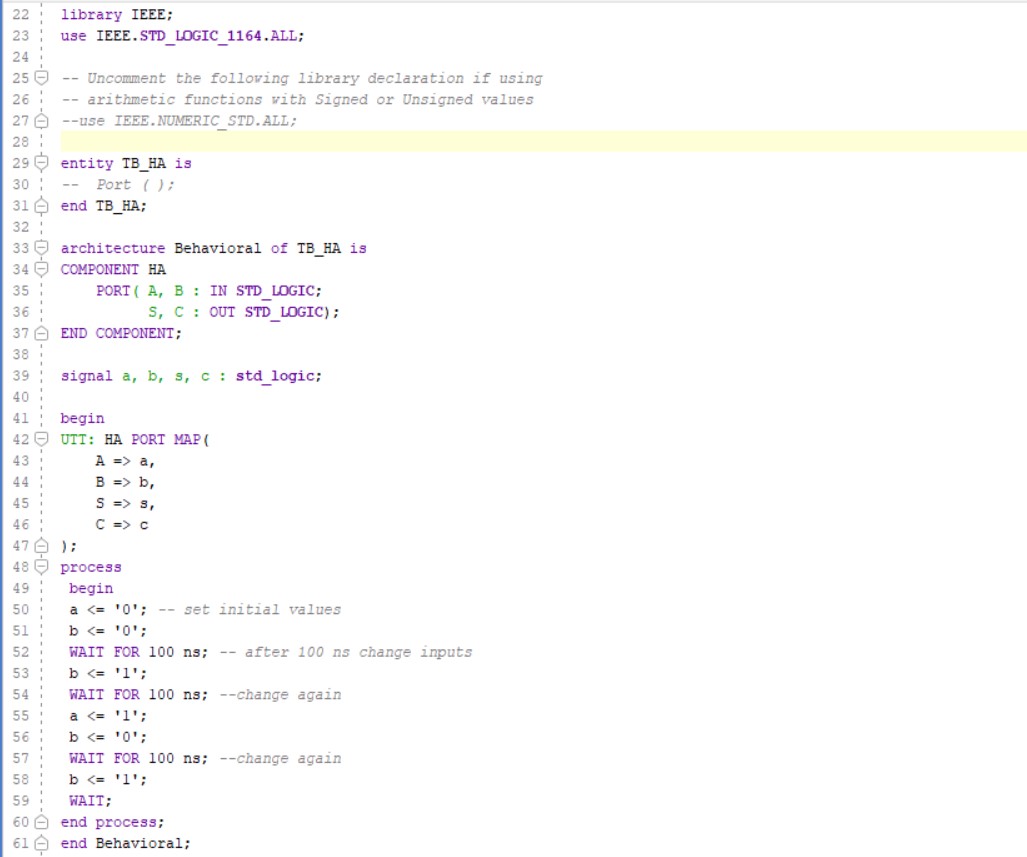


3). 4-Bit RCA

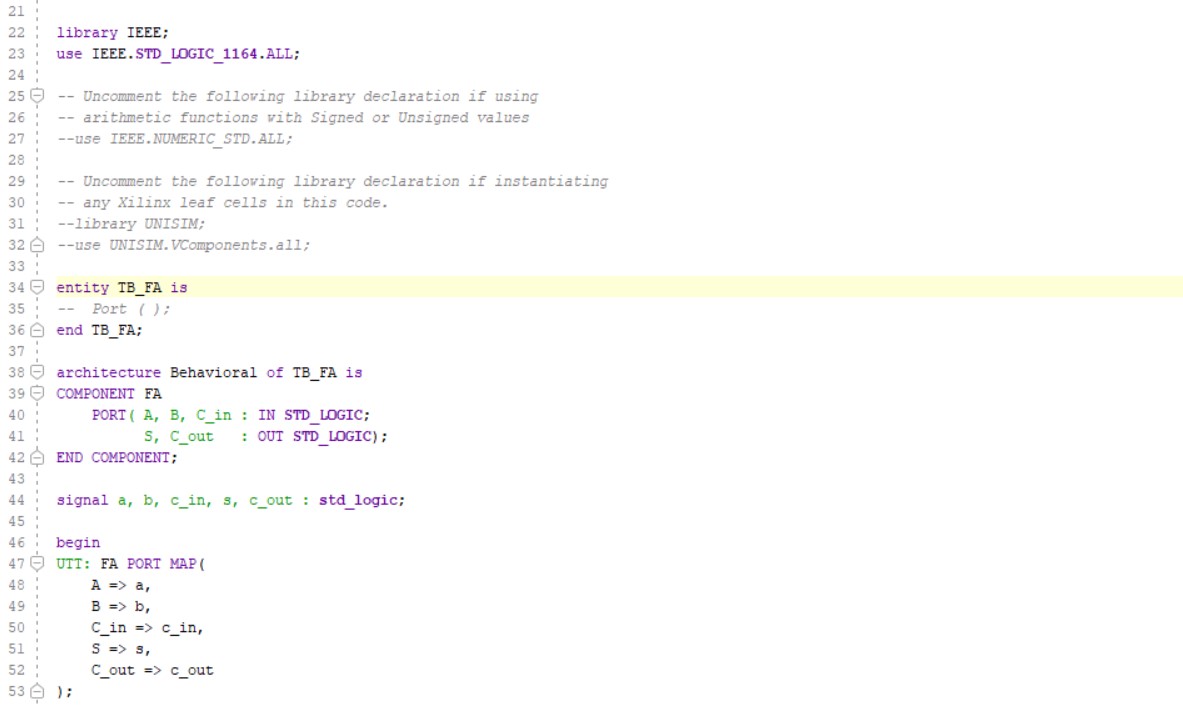


Test Bench Files: -

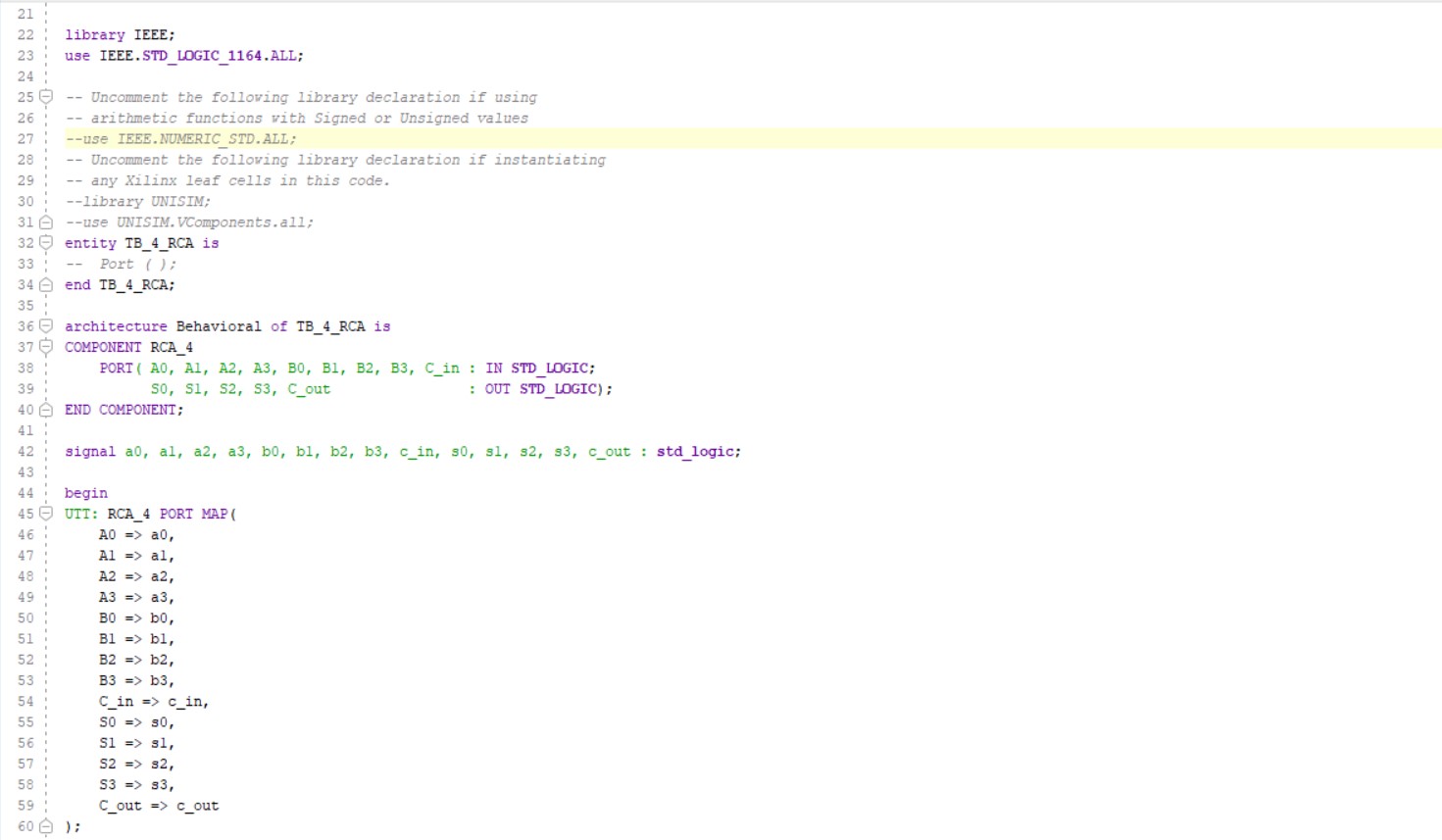
1). Half Adder



2). Full Adder



3). 4 – Bit RCA



Discussion :

* Why some of the input combinations results in outputs that cannot be represented using LED LD0-LD3?

Inputs ranging from 0 to 15 can be provided from SW0 to SW3 or SW12 to SW15. As a result, the output will fall between 0 and 30. However we can only indicate outputs in range of 0 to 15 using LD0 - LD3.

* Discuss the role of LD15

The aim of LD15 is to show the overflow that we obtain from the numbers in the range of 16 to 30, as we can only output values from 0 to 15.

Conclusions :

Fundamental circuits are used to construct even the most complicated circuits. In this lab, the Half Adder was utilized to create a Full Adder and a 4-Bit Ripple Carry Adder. Furthermore, we bundled our IP for next developments.